UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,966	09/11/2003	Jerry Chuang	X-1440 US	5036

24309	7590	09/12/2006

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER
TRAN, PABLO N

ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 09/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/659,966	CHUANG ET AL.
	Examiner	Art Unit	
	Pablo N. Tran	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _26 June 2006_.
2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-41_ is/are pending in the application.
    4a) Of the above claim(s) _14-41_ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) _1-6 and 9-13_ is/are rejected.
7) ☒ Claim(s) _7 and 8_ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a) ☐ All   b) ☐ Some * c) ☐ None of:
        1. ☐ Certified copies of the priority documents have been received.
        2. ☐ Certified copies of the priority documents have been received in Application No. _____.
        3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)
1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _01/16/04_.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____ .

DETAILED ACTION

Election/Restrictions

1.   Claims 14-41 withdrawn from further consideration pursuant to 37 CFR 1.142(b),

as being drawn to a nonelected Group II-V there being no allowable generic or linking

claim. Applicant timely traversed the restriction (election) requirement in the reply filed

on 06/26/06.

2.   This application contains claims 14-41 drawn to an invention nonelected with

traverse in examiner's action filed on 06/13/06. A complete reply to the final rejection

must include cancellation of nonelected claims or other appropriate action (37

CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 102

3.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4.   Claims XX are rejected under 35 U.S.C. 102(b) as being anticipated by

Vanderspool, II et al. (5,398,263).

As per claim 1, Vanderspool, II et al. disclose a transceiver for processing high

data rate serial data, having a phase-locked loop circuitry (fig. 7) further including

selectable coarse loop PLL and selectable fine loop PLL circuits, the selectable coarse

loop PLL for producing a coarse loop synchronized oscillation signal based on a

reference clock, the coarse loop synchronized oscillation signal having a specified

degree of accuracy relative to a received serial data rate and the selectable fine loop

PLL for adjusting the coarse loop synchronized oscillation signal to further synchronize

with the received high data rate serial data; and mode determination logic coupled to

produce mode switching signals to selectively switch the selectable coarse loop PLL

and selectable fine loop PLL into and out of coupling according to defined operational

logic within the mode determination logic (abstract, fig. 7, fig. 8, fig. 10, col. 4/ln. 29-col.

4/ln. 11, col. 8/ln. 39-56, col. 9/ln. 23-49).

As per claim 2, Vanderspool, II et al. disclose the mode determination logic

produces the mode switching signals responsive to one of an automatic mode, a

sample mode, and a receive mode of operation (col. 4/ln. 29-col. 4/ln. 11, col. 8/ln. 39-

56, col. 9/ln. 23-49).

As per claim 3, Vanderspool, II et al. disclose when in the automatic mode of

operation, further operates according to an initial (coarse) calibration mode of operation

and a final (fine) calibration mode of operation (col. 4/ln. 29-col. 4/ln. 11, col. 8/ln. 39-56,

col. 9/ln. 23-49).

As per claim 4, Vanderspool, II et al. disclose when in the initial calibration mode,

selectively de-couples the selectable fine loop PLL and couples the selectable coarse

loop PLL (col. 4/ln. 29-col. 4/ln. 11, col. 8/ln. 39-56, col. 9/ln. 23-49).

As per claim 5, Vanderspool, II et al. disclose selectively couples the selectable fine loop PLL after a specified period (col. 4/ln. 29-col. 4/ln. 11, col. 8/ln. 39-56, col. 9/ln. 23-49).

As per claim 6, Vanderspool, II et al. disclose selectively de-couples the selectable coarse loop PLL (col. 4/ln. 29-col. 4/ln. 11, col. 8/ln. 39-56, col. 9/ln. 23-49).

As per claim 9, Vanderspool, II et al. disclose the automatic mode of operation is a default mode of operation (col. 4/ln. 29-col. 4/ln. 11, col. 8/ln. 39-56, col. 9/ln. 23-49).

As per claim 10, Vanderspool, II et al. disclose the mode determination logic operates according to the automatic mode of operation responsive to a mode selection signal received from an external source (col. 4/ln. 29-col. 4/ln. 11, col. 8/ln. 39-56, col. 9/ln. 23-49).

As per claim 11, Vanderspool, II et al. disclose when in the sample mode of operation, selectively de-couples the selectable fine loop PLL and couples the selectable coarse loop PLL as long as the transceiver is in the sample mode of operation (col. 4/ln. 29-col. 4/ln. 11, col. 8/ln. 39-56, col. 9/ln. 23-49).

As per claim 12, Vanderspool, II et al. disclose the phase-locked loop circuitry to lock to a local reference for data sampling operations responsive to the mode selection signal received from the external source (col. 4/ln. 29-col. 4/ln. 11, col. 8/ln. 39-56, col. 9/ln. 23-49).

As per claim 13, Vanderspool, II et al. disclose the phase-locked loop circuitry to lock to the received serial data rate responsive to the mode selection signal received from the external source (col. 4/ln. 29-col. 4/ln. 11, col. 8/ln. 39-56, col. 9/ln. 23-49).

Allowable Subject Matter

5.   Claims 7-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pablo Tran whose telephone number is (571)272-7898. The examiner normal hours are 9:30 -5:00 (Monday-Friday). If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban, can be reached at (571)272-7899. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

7.   Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) System. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see httpr//pair-directauspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

September 5, 2006

PABLO N. TRAN
PRIMARY EXAMINER